AMENDMENTS TO THE CLAIMS

1 - 46. canceled

47. (previously presented) A wafer-level chip scale package, comprising:

a substrate containing a chip pad;

a re-distributed line (RDL) pattern on the chip pad;

an insulating layer covering a portion of the RDL pattern, wherein the insulating layer comprises a non-polymeric dielectric material;

a stud bump located on the portion of the RDL pattern not covered by the insulating layer;

a leadframe substrate containing a bond pad; and

an adhesive material containing conductive particles located between the substrate and the leadframe substrate, wherein the conductive particles comprise metal with an insulating layer.

48. (previously presented) The package of claim 47, wherein at least one conductive particle is located between the stud bump and the bond pad.

49. (previously presented) The package of claim 47, wherein the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste.

50. (previously presented) The package of claim 47, wherein the package does not contain any solder paste.

51. (previously presented) The package of claim 47, wherein the stud bump comprises Cu.

52. (previously presented) The package of claim 47, wherein the stud bump is formed by wire bonding a Pd coated copper wire to the RDL pattern using a capillary to provide the stud bump with a coined shape.

53. (previously presented) The package of claim 47, wherein the insulating layer comprises silicon nitride, silicon oxide, or silicon oxynitride.

54. (previously presented) The package of claim 47, wherein there is no under bump metal under the stud bump.

55. (previously presented) A wafer-level chip scale package, comprising:

a substrate containing a chip pad;

a re-distributed line (RDL) pattern on the chip pad;

an insulating layer covering a portion of the RDL pattern, wherein the insulating layer comprises a non-polymeric dielectric material;

a Cu-containing stud bump located on the portion of the RDL pattern not covered by the insulating layer;

a leadframe substrate containing a bond pad; and

an adhesive material containing conductive particles located between the substrate and the leadframe substrate with at least one conductive particle contacting both the stud bump and the bond pad, wherein the conductive particles comprise metal with an insulating layer.

56. (previously presented) The package of claim 55, wherein the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste.

57. (previously presented) The package of claim 55, wherein the package does not contain any solder paste.

58. (previously presented) The package of claim 55, wherein the insulating layer comprises silicon nitride, silicon oxide, or silicon oxynitride.

59. (previously presented) The package of claim 55, wherein there is no under bump metal under the stud bump.

60. (previously presented) The package of claim 55, wherein the stud bump is formed by wire bonding a Pd coated copper wire to the RDL pattern using a capillary to provide the stud bump with a coined shape.

61. (previously presented) A wafer-level chip scale package, comprising:

a substrate containing an integrated circuit;

a re-distributed line (RDL) pattern on the substrate and the integrated circuit;

an insulating layer covering a portion of the RDL pattern, wherein the insulating layer comprises a non-polymeric dielectric material;

a non-reflowed stud bump located on the portion of the RDL pattern not covered by the insulating layer;

a leadframe substrate containing a bond pad; and

an adhesive material containing conductive particles located between the substrate and the leadframe substrate.

62. (previously presented) The package of claim 61, wherein the conductive particles comprise metal with an insulating layer.

63. (previously presented) The package of claim 61, wherein the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste.

64. (previously presented) The package of claim 61, wherein the package does not contain any solder paste.

65. (previously presented) The package of claim 61, wherein the stud bump comprises Cu.

66. (previously presented) The package of claim 61, wherein there is no under bump metal under the stud bump.

67. (previously presented) An electronic apparatus containing a packaged semiconductor device without solder paste, the device comprising:

a substrate containing a chip pad;

a re-distributed line (RDL) pattern on the chip pad;

an insulating layer covering a portion of the RDL pattern, wherein the insulating layer comprises a non-polymeric dielectric material;

a Cu-containing stud bump located on the portion of the RDL pattern not covered by the insulating layer;

a leadframe substrate containing a bond pad; and

an adhesive material containing conductive particles located between the substrate and the leadframe substrate with at least one conductive particle contacting both the stud bump and the bond pad, wherein the conductive particles comprise metal with an insulating layer.

68. (previously presented) The apparatus of claim 67, wherein the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste.

69. (previously presented) The apparatus of claim 67, wherein the package does not contain any solder paste.

70. (previously presented) The apparatus of claim 67, wherein the insulating layer comprises silicon nitride, silicon oxide, or silicon oxynitride.

71. (previously presented) The apparatus of claim 67, wherein there is no under bump metal under the stud bump.

72. (currently amended) The apparatus of claim 67, wherein the ~~package does not contain any solder paste~~ substrate comprises a BT epoxy material.